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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/619,477	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-33,35-44 and 46-58* is/are pending in the application.

4a) Of the above claim(s) *54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-33,35-44,46-53 and 55-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 6 August 2004 and the IDS filed 13 August 2004.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **31**-33, 35, 39, 42, 55, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,169,593 B1 (**Kanaya** et al.) in view of JP 9-251996 (**Yamazaki** et al.).

Regarding claim 31, **Kanaya** discloses a semiconductor device which is a liquid crystal display --as further limited by instant claim 42-- comprising

a first substrate **20**;

a first circuit comprising a thin film transistor (TFT) formed comprising a semiconductor film (col. 7, lines 40-53; col. 8, lines 43-46) formed over said first substrate;

a second substrate (Fig. 4A called "a driving circuit board **21**" col. 9, lines 17-39) opposing said first substrate **20**;

a second circuit under said second substrate **21**;

a connecting wiring for electrically connecting said first circuit and said second circuit, said connecting wiring comprising,

a metallic film **22** (gate signal wire; col. 8, lines 25-29) formed over the first substrate **20**; and

a transparent conductive film (TCF) **28** (source signal wire; col. 8, ll. 50-51) over said metallic film **22**; and

a insulating film **24** in contact with a side surface of said metallic film and formed along with a longer side and a shorter side of the metallic film **22** --as further limited by instant claim 57. (See Figs. 2G and 2H; col. 9, ll. 13-40. See also col. 18, ll. 24-51 and Figs. 15A-15B.) Note the protecting film **24** is the same film insulating between **22** and **28** as shown in Fig. 2F --as further limited by instant claim 32.

In another embodiment as shown in Figs. 7E-7F, **Kanaya** discloses the metal film **26** of about 300 nm (col. 13, lines 37-40) with overlying TCF **28** of a thickness of about 70 nm (col. 9, line 25) --as further limited by instant claim 35-- and protecting film **30** formed of, for example, an acrylic resin and formed along the length and width direction of the lamination film and contacting a side surface of the metal film **26**. (See also col. 14 -- esp. ll. 7-10, 45-67; Figs 12D, 13B.)

Kanaya does not teach that the wiring has a tapered shape.

Yamazaki teaches that contact holes are conventionally required to be tapered to improve the step coverage of upper-layer wiring lines at contact holes (paragraph [0003] first sentence).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the connecting wiring of **Kanaya** to have a tapered shape, as taught in **Yamazaki** because **Yamazaki** teaches that tapering is conventional and required to improve step coverage. Note whether the insulating material deposited on the tapered wiring or the wiring is deposited

over a tapered opening in the insulating material and therefore takes on the tapered shape, the tapered shape contributes to better step coverage, as taught by **Yamazaki**.

Regarding claim 33, **Kanaya** shows the first and second circuits of the first and second substrates, respectively, are connected via an anisotropic conductive film **80a** (Fig. 2H; also called "output terminal" in Figs. 4A-4B).

Regarding claim 55, **Kanaya** discloses the lamination film is formed of the same materials as the source and drain wiring. (See col. 13, lines 32-36 and especially the paragraph bridging cols. 14-15.)

3. Claims **31**-33, 35-37, 42, 55, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,636,329 (**Sukegawa** et al) in view of JP 9-251996 (**Yamazaki** et al.).

The prior art Fig. 2A-2C of **Sukegawa** showing a terminal portion of an LCD display discloses a first substrate **1**;

a first circuit comprising a thin film transistor (TFT) comprising a semiconductor film **4**;

a second substrate (called a "tape carrier package **300** as a driver IC" Fig. 3D; col. 5, lines 27-44) opposing said first substrate **1**;

a second circuit under said second substrate **300** (Fig. 3D);

a connecting wire for electrically connecting said first circuit and said second circuit, said connecting wiring comprising,

a metallic film **7** over said first substrate **1**, and

a transparent conductive film (TCF) **8** of 40 nm thick (col. 5, lines 6-10) over and in contact with the metallic film surface **7** for connecting said circuit structured with a TFT to

another circuit using an anisotropic conductive film (ACF) **10** --as further limited by instant claim 33--;

an insulating film **3** in contact with a side surface of said metallic film **7**, wherein said insulating film **7** is formed along with a longer side and a shorter side of the metallic film --as further limited by instant claim 57. (See also col. 3, ll. 9-33 and prior art Figs. 1A-1B.)

Fig. 4A-4B of **Sukegawa** discloses a first substrate **1** having a circuit structured with a thin film transistor (TFT); a second substrate **200** opposing said first substrate **1**; a connecting wire formed of a metallic film **7** formed 140 nm thick from Cr, Al, W, etc. (col. 8, ll. 59-63) and a transparent conductive film (TCF) **8** in contact with the metallic film surface for connecting said circuit structured with a TFT (Fig. 3C) to another circuit using an anisotropic conductive film (ACF) **10**; and a protecting film **3** in contact with a side surface of said metallic film **7**, wherein said connecting wiring and said protecting film **7** are formed over said first substrate **1**, and formed along the length direction of the lamination film. Note also that at col. 7, ll. 40-44, **Sukegawa** states, "That is, the upper layer metal wiring **7** is protected at least by double coverage with a transparent conductive film **10** and further protected, locally, by coverage with a protective insulation film **9**. (See also col. 3, ll. 9-33 and prior art Figs. 1A-1B.)

Sukegawa does not teach that the wiring has a tapered shape.

Yamazaki teaches that contact holes are conventionally required to be tapered to improve the step coverage of upper-layer wiring lines at contact holes (paragraph [0003] first sentence).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the connecting wiring of **Sukegawa** to have a tapered shape, as taught in **Yamazaki** because **Yamazaki** teaches that tapering is conventional and required to improve step coverage.

Regarding claim 33, **Sukegawa** discloses the connection wiring is connected to a wiring **31a**, **31b** of a third substrate via an anisotropic conductive film (Fig. 3E).

Regarding claim 55, **Sukegawa** discloses the lamination film is formed of the same materials as the source and drain wiring. (See Fig. 3C and associated text.)

4. Claims **31**-33, 35-37, 39, 42, 55, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,608,559 (**Inada** et al.) in view of JP 9-251996 (**Yamazaki** et al.).

The prior art Figs. 1-2 of **Inada,** showing a terminal portion of an LCD panel, discloses

a first substrate **221**;

a first circuit comprising a thin film transistor (TFT) comprising a semiconductor film **306** (Fig. 14);

a second substrate **204** opposing said first substrate **221** which is a flexible wiring substrate;

a second circuit **224** under the second substrate;

a connecting wire for electrically connecting said first circuit and said second circuit, said connecting wiring comprising

a 300-nm thick metallic film **209** formed over the first substrate, and

an 80-nm thick transparent conductive film (TCF) **210** over and in contact with the metallic film surface for connecting said circuit structured with a TFT to another circuit using an anisotropic conductive film (ACF) **211**; and

an insulating film **211** covering a side surface of said metallic film **209**, wherein said insulating film **211** is formed along with a longer side and a shorter side of the metallic film --as further limited by instant claim 57.

(See col. 1, ll. 29-34.)

Fig. 6 of **Inada** discloses a similar embodiment to the prior art figure but shows the protective film **42** of silicon nitride on the side of, and formed along the length and width direction of, the lamination film formed of the 300-nm thick metal film **29** with overlying 80-nm thick transparent conductive film **30** and anisotropic conductive film **36** (col. 8, ll. 50-51). (See also col. 7, ll. 10-30; col. 14, ll. 32-42; col. 4, ll. 24-34).

Inada does not teach that the wiring has a tapered shape.

Yamazaki teaches that contact holes are conventionally required to be tapered to improve the step coverage of upper-layer wiring lines at contact holes (paragraph [0003] first sentence).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the connecting wiring of **Inada** to have a tapered shape, as taught in **Yamazaki** because **Yamazaki** teaches that tapering is conventional and required to improve step coverage. Note whether the insulating material deposited on the tapered wiring or the wiring is deposited over a tapered opening in the insulating material and therefore takes on the tapered shape, the tapered shape contributes to better step coverage, as taught by **Yamazaki**.

Regarding claim 32, **Inada** discloses that protective film **310** between source/drain wiring is that same as protective film **42** which are each SiN (Fig. 14; col. 14, lines 32-42).

Regarding claim 33, **Inada** discloses the first and second circuits are connected via an anisotropic conductive film **211** (Fig. 2), **36** (Fig. 6).

Regarding claim 55, **Inada** discloses the lamination film is formed of the same materials as the source and drain wiring. (See Fig. 14 and associated text.)

5. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over any of **Kanaya** in view **Yamazaki**, **Sukegawa** in view **Yamazaki**, and **Inanda** in view **Yamazaki**, each as applied to claim 31 above, and further in view of US 5,821,159 (**Ukita**).

Each of **Kanaya** in view **Yamazaki**, **Sukegawa** in view **Yamazaki**, and **Inanda** in view **Yamazaki**, as explained above, teaches each of the features of the claims except for forming the metallic film as a laminate of tungsten W and tungsten nitride compound WN_X. **Kanaya** does however teach an example of another refractory metallic film as a laminate of tantalum/tantalum nitride or Ta/TaN (col. 17, ll. 44-48).

Ukita discloses that it is known in the LCD art to make a metallic film for an interconnection wiring as a laminate of a tungsten and its nitride (col. 4, lines 21-25). It has been held that selection of a known material based on its suitability for its intended use is *prima facie* obvious. See Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 1945). See also In re LESHIN, 125 USPQ 416 (CCPA 1960).

It would have been obvious to one of ordinary skill at the time of the invention to use a tungsten and its nitride to form the metallic film of any of **Kanaya**, **Sukegawa**, and **Inada** as

taught in **Ukita** because, in the case of **Kanaya, Kanaya** discloses a similar laminate of another refractory metal and because tungsten and its nitride would be expected to work just as well as the other metallic films for interconnect wiring, according to precedent.

6. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over any of **Kanaya** in view **Yamazaki**, **Sukegawa** in view **Yamazaki**, and **Inanda** in view **Yamazaki**, each as applied to claim 31 above, and further in view of US 6,215,077 B1 (**Utsumi** et al.).

Each of **Kanaya** in view **Yamazaki**, **Sukegawa** in view **Yamazaki**, and **Inanda** in view **Yamazaki**, as explained above, teaches each of the features of the claims except for forming the transparent conductive film from zinc oxide and compounds of zinc oxide and indium oxide.

Utsumi teaches the benefits of using a laminate of a metallic film 2b, 2c comprising aluminum layer 2b with overlying IZO 2a specifically for use on transparent substrates for LCDs. (See Abstract, col. 2, l. 45 to col. 3, l. 16; and especially col. 4, ll. 49-58.)

It would have been obvious to one of ordinary skill at the time of the invention to use the metallization scheme of **Utsumi** for the reasons in **Utsumi** -- at least to form a metallization free from hillocks which has a low resistance even though it incorporates a conductive metal oxide.

Moreover, it has been held that selection of a known material based on its suitability for its intended use is *prima facie* obvious. See Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 1945). See also In re LESHIN, 125 USPQ 416 (CCPA 1960). It would have been obvious to one of ordinary skill at the time of the invention to use zinc oxide or zinc oxide and indium oxide to form the transparent conductive film of any of **Kanaya**, **Sukegawa**, and **Inada** as taught in **Utsumi** because either material would be expected to work

just as well as the transparent conductive films of each of **Kanaya**, **Sukegawa**, and **Inada** for interconnect wiring, according to precedent.

7. Claims **43**, 44, 46, 50, 53, 56, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kanaya** in view of **Yamazaki** and JP 8-234212 A (**Hioki**).

Kanaya in view of **Yamazaki**, as explained above, teaches each of the features of the claims except for forming column-shaped spacers over the TFTs, wherein the material used to form the spacers is the same material as that used to form the protective film.

Hioki teaches the benefits of forming column-shaped spacers **24** over the TFTs **22** using a resin. It would have been obvious to one of ordinary skill at the time of the invention to form spacers over the TFTs of **Hioki** and form them from resin for the reasons indicated in **Hioki** -- especially because forming the spacers over the TFTs provides uniform light over the pixels.

Because **Kanaya** teaches embodiments wherein the protecting film material is made from resin, both the spacers and the protecting film are formed from the same material.

8. Claims **43**, 44, 46-48, 53, 56, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sukegawa** in view of **Yamazaki** and **Hioki**.

Sukegawa in view of **Yamazaki**, as explained above, teaches each of the features of the claims except for forming column-shaped spacers over the TFTs, wherein the material used to form the spacers is the same material as that used to form the protective film.

Hioki teaches the benefits of forming column-shaped spacers **24** over the TFTs **22** using a resin. It would have been obvious to one of ordinary skill at the time of the invention to form

spacers over the TFTs of **Hioki** and form them from resin for the reasons indicated in **Hioki** -- especially because forming the spacers over the TFTs provides uniform light over the pixels.

Because **Sukegawa** teaches embodiments wherein the protecting film material is made from resin, both the spacers and the protecting film are formed from the same material.

9. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over any of **Kanaya** in view **Yamazaki** and **Hioki**, **Sukegawa** in view **Yamazaki** and **Hioki**, and **Inanda** in view **Yamazaki** and **Hioki**, each as applied to claim 43 above, and further in view of US 5,821,159 (**Ukita**).

Each of **Kanaya** in view **Yamazaki** and **Hioki**, **Sukegawa** in view **Yamazaki** and **Hioki**, and **Inanda** in view **Yamazaki** and **Hioki**, as explained above, teaches each of the features of the claims except for forming the metallic film as a laminate of tungsten W and tungsten nitride compound WN_X. **Kanaya** does however teach an example of another refractory metallic film as a laminate of tantalum/tantalum nitride or Ta/TaN (col. 17, ll. 44-48).

Ukita discloses that it is known in the LCD art to make a metallic film for an interconnection wiring as a laminate of a tungsten and its nitride (col. 4, lines 21-25). It has been held that selection of a known material based on its suitability for its intended use is *prima facie* obvious. See Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 1945). See also In re LESHIN, 125 USPQ 416 (CCPA 1960).

It would have been obvious to one of ordinary skill at the time of the invention to use a tungsten and its nitride to form the metallic film of any of **Kanaya**, **Sukegawa**, and **Inada** as taught in **Ukita** because, in the case of **Kanaya, Kanaya** discloses a similar laminate of another

refractory metal and because tungsten and its nitride would be expected to work just as well as the other metallic films for interconnect wiring, according to precedent.

10. Claims 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over any of **Kanaya** in view **Yamazaki** and **Hioki**, **Sukegawa** in view **Yamazaki** and **Hioki**, and **Inanda** in view **Yamazaki** and **Hioki**, each as applied to claim 43 above, and further in view of US 6,215,077 B1 (**Utsumi** et al.).

Each of **Kanaya** in view **Yamazaki** and **Hioki**, **Sukegawa** in view **Yamazaki** and **Hioki**, and **Inanda** in view **Yamazaki** and **Hioki**, as explained above, teaches each of the features of the claims except for forming the transparent conductive film from zinc oxide and compounds of zinc oxide and indium oxide.

Utsumi teaches the benefits of using a laminate of a metallic film 2b, 2c comprising aluminum layer 2b with overlying IZO 2a specifically for use on transparent substrates for LCDs. (See Abstract, col. 2, l. 45 to col. 3, l. 16; and especially col. 4, ll. 49-58.)

It would have been obvious to one of ordinary skill at the time of the invention to use the metallization scheme of **Utsumi** for the reasons in **Utsumi** -- at least to form a metallization free from hillocks which has a low resistance even though it incorporates a conductive metal oxide.

Moreover, it has been held that selection of a known material based on its suitability for its intended use is *prima facie* obvious. See Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 1945). See also In re LESHIN, 125 USPQ 416 (CCPA 1960). It would have been obvious to one of ordinary skill at the time of the invention to use zinc oxide or zinc oxide and indium oxide to form the transparent conductive film of any of **Kanaya**,

Sukegawa, and **Inada** as taught in **Utsumi** because either material would be expected to work just as well as the transparent conductive films of each of **Kanaya**, **Sukegawa**, and **Inada** for interconnect wiring, according to precedent.

Response to Arguments

11. Applicant's arguments filed 6 August 2004 have been fully considered but they are not persuasive.

Applicant comments that Examiner is not addressing the arguments regarding the motivation to combine the references. As an initial matter, Examiner is not required to address arguments when arguments are moot in view of new grounds of rejection. In any case, the motivation to combine the references is and always has been proper and is stated above in the rejection of the claims. The motivation to combine the references is further clarified.

In this regard, Applicant argued in the Response filed 17 March 2004 that because Yamazaki (JP 9-251996) teaches only that an opening in an insulating layer is tapered to improve the step coverage of a metal deposited therein and thereover, that one of ordinary skill would not recognize that inverting the material layers, i.e. depositing the insulating material over a patterned metal layer, that the same better step coverage and therefore better insulating properties would be obtained. Examiner respectfully disagrees. Note it has been held that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968) See also *In re Lamberti*, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976).

As proof that it would be known to one of ordinary skill in the art from the Yamazaki teaching that it does not matter whether metal is deposited over tapered openings in an insulating layer or vice versa (i.e. insulation over tapered wiring openings) consider the numerous examples of proof:

(1) US 5,897,377 (**Suzuki**) teaches that it is notoriously well known in the art that (i.e. is stated in the section entitled "Description of Related Art"), that there exists an equivalence between depositing metal over tapered insulation or vice versa. In this regard, **Suzuki** states at col. 1, last paragraph,

> "In addition, in the etching process, vertical etching is not always most desirable. For example, a **wiring pattern** should preferably be etched in a normal **taper** manner in order to **improve the coverage** of an interlayer insulating film, **and also**, a **contact-hole or via-hole** should be etched in a normal **taper** manner in order to **improve the coverage** of a metallic wiring pattern in the hole." (Emphasis added.)

Accordingly, the **Yamazaki** reference alone is clearly sufficient of a teaching to one of ordinary skill that to taper the metal layer, as expressly shown to be true in **Suzuki**.

(2) US 4,352,724 (**Sugishima** et al.) teaches the same equivalency as does **Sukzuki**. (See Sugushima at col. 7, lines 41-47.) Again, the **Yamazaki** reference alone is clearly sufficient of a teaching to one of ordinary skill that to taper the metal layer, as expressly taught in **Sugushima**.

(3) Each of the following references teaches forming tapered wiring to improve step coverage of the insulating film formed thereover and thereby improves the wiring reliability, again pointing out the equivalency that it does not matter which material is deposited first, as long as the lower of the two is tapered so as to provide a tapered wiring layer directly or indirectly:

US 5,668,379 (**Ono** et al.), Fig. 3; col. 8, lines 55-63 and col. 9, lines 52-65. Note additionally that **Ono** teaches that an ITO layer deposited over a tapered metal wiring layer prevents breakage of the ITO layer --yet another benefit directly applicable to any of **Kanaya**, **Sukegawa**, and **Inanda**.

US 5,913,100 (**Kohsaka** et al.) col. 4, lines 50-63.

JP 57-147253 A (**Katsuyama**) Abstract, Figs. 2a-2c.

JP 59-28344 A (**Ikeyama**) Abstract, Figs. 1-5.

JP 63-161645 A (**Tsubakiyama**) Abstract, Figs. 1a-1h, 2.

JP 02-244631 A (**Ito**) Abstract.

For at least these reasons, Examiner respectfully submits that the motivation to combine **Yamazaki** with each of **Kanaya**, **Sukegawa**, and **Inanda** to form tapered wiring layers, either directly or indirectly is proper because it gives better step coverage of the insulating wire by having the wire tapered or, alternatively, to give a tapered wiring of better coverage and reliability over a tapered opening in an insulating layer. Accordingly, the combination as originally presented is still considered proper.

Further in this regard, Applicant has argued that each of **Kanaya**, **Sukegawa**, and **Inanda** is drawn to depositing insulating films over metal. While it is acknowledged that **Kanaya** and **Inanda** do this and, as stated above is still irrelevant given the teaching in **Yamazaki** to form the wiring in a tapered shape to improve step coverage of the insulating layer, **Sukegawa** does not teach this. Rather **Sukegawa** teaches depositing metal 7 in insulating layer 3. Accordingly, Applicant's arguments regarding the combination of **Yamazaki** with **Sukegawa** are not in concert with the teachings is **Sukegawa**. In this regard, it is not the responsibility of

the Office to point out repeatedly that which is clearly shown in the reference itself, even though the Office has repeatedly pointed this out in each citation of the **Sukegawa** reference.

For at least these reasons, Applicant's arguments are not persuasive of novelty and non-obviousness of the instant claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Each of the following references teaches the benefits of depositing a metal layer in a tapered opening to form a tapered wiring having improved wiring reliability:

JP 55-98832 A (**Kauchi**) Abstract, Figs. 1A, 2A.

JP 59-214228 A (**Okada** et al.) Abstract, Figs. 2d, 3.

JP 04-333224 A (**Hoshi**) Abstract, Fig. 1c.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

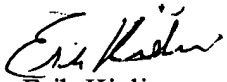
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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20 October 2004